REMARKS

Claims 1-14 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Kudo et al. (U.S. Patent 6,560,692). This rejection is respectfully traversed for the following reasons.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989). The term "anticipation," in the sense of 35 U.S.C. § 102, has acquired the accepted definition meaning "the disclosure in the prior art of a thing substantially identical with the claimed invention." ***In re Schaumann***, 572 F.2d 312, 197 USPQ 5 (CCPA 1978).

Claim 1 recites a microprocessor including:

- a program control unit controlling fetch of an instruction code;

- an instruction decode unit decoding said fetched instruction code;

- an address operation unit operating an address of a memory on the basis of the result of decoding by said instruction decode unit; and

- a data operation unit operating data on the basis of the result of decoding by said instruction decode unit.

The claim specifies that the data operation unit executes data transfer between registers and data transfer between said registers and said memory in correspondence to single said instruction code having a single operation code fetched by said program control unit.

The Examiner relies upon col. 14, lines 44-53, col. 15, lines 20-28, col. 25, lines 29-67, and col. 26, lines 30-35 of Kudo et al. for disclosing the transfer between registers and transfer between registers and memory in response to a single instruction code.

Considering the reference, Kudo et al. discloses sequentially transferring data from general-purpose registers R0-R3 to memory stack (col. 15, lines 20-28, col. 25, lines 29-67). The reference indicates that when data is transferred between a special register and the stack, they are transferred via a general-purpose register (col. 26, lines 30-35). Also, Kudo et al. discloses that stack pointer instructions to access a stack-pointer register (SP) comprise instructions branching to other routines (col. 14, lines 44-53).

However, none of the portions of Kudo et al. relied upon by the Examiner discloses transfer between registers and transfer between the registers and a memory in correspondence to a single instruction code having a single operation code, as claim 1 requires.

In the event the Examiner relied upon inherency without expressly indicating such reliance, the Examiner should be aware that inherency requires certainty, not speculation. ***In re Rijckaert***, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); ***In re King***, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); ***W. L. Gore & Associates, Inc. v. Garlock, Inc.***, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); ***In re Oelrich***, 666 F.2d 578, 212 USPQ 323 (CCPA 1981); ***In re Wilding***, 535 F.2d 631, 190 USPQ 59 (CCPA 1976). To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. ***In re Robertson***, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

It is respectfully submitted that the Examiner provided no factual basis upon which to conclude that the transfer between registers and transfer between the registers and the memory described in the reference are carried out in the manner required by claim 1, i.e., in correspondence to a single instruction code having a single operation code.

Accordingly, it cannot be said that Kudo et al. describes the claimed invention within the meaning of 35 U.S.C. § 102.

Independent claim 11 recites an assembler including:

- a code reading unit reading a code from a source program;

- a storage unit storing information for specifying a plurality of registers;

- a first code generation unit storing said information for specifying said plurality of registers included in said code read by said code reading unit in said storage unit and generating a code to push data stored in said plurality of registers when said code is a first macro instruction; and

- a second code generation unit referring to said information for specifying said plurality of registers stored in said storage unit and generating a code to pop data stored in said plurality of registers when said code read by said code reading unit is a second macro instruction.

The Examiner relies upon col. 17, lines 5-16 for disclosing the claimed first and second code generation units. It is noted that this portion of the reference discloses an instruction set including instruction codes (1) to (8) created by an assembler to transfer data of various length between a register and the stack.

However, Kudo does not disclose storing information for specifying a plurality of registers in a code and referring to this information for generating a code to push data from the plurality of registers, as claim 11 recites. Also, the reference does not disclose generating a code to pop data stored in the plurality of registers.

Independent claim 13 recites a storage medium, readable by a computer, on which an assembly program for making said computer execute an assembly method is recorded. The assembly method comprises the steps of:

- reading a code from a source program;

- storing information for specifying a plurality of registers included in said code and generating a code to push data stored in said plurality of registers when said code is a first macro instruction; and

- referring to said stored information for specifying said plurality of registers and generating a code to pop data stored in said plurality of registers when said read code is a second macro instruction.

As discussed above, Kudo does not disclose the claimed steps of storing information for specifying a plurality of registers included in said code and generating a code to push data stored in said plurality of registers when said code is a first macro instruction; and referring to said stored information for specifying said plurality of registers and generating a code to pop data stored in said plurality of registers when said read code is a second macro instruction.

Moreover, the reference provides no reason for one skilled in the art to conclude that Kudo et al. inherently carries storing information for specifying a plurality of registers in a code and referring to this information to generate a code to push data from the plurality of registers. Hence, Kudo et al. neither expressly nor inherently discloses the inventions recited in claims 11 and 13.

The dependent claims 2-10, 12 and 14 are defined over the reference at least for the reasons presented above in connection with the respective independent claims.

Applicants, therefore, respectfully submit that the rejection of claims 1-14 under 35 U.S.C. § 102 as anticipated by Kudo et al. is untenable and should be withdrawn.

In view of the foregoing, and in summary, claims 1-14 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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